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14. ABSTRACT More than forty years ago, Professor Chua predicted the existence of the memristor to complete the set of passive devices that previously includes only resistor, capacitor, and inductor. However, till 2008 the first physical realization of memristors was demonstrated by HP Lab. The unique properties of memristor create great opportunities in future system design. For instance, the memristor has demonstrated the similar function as synapse, which makes it promising to utilize memristor in neuromorphic circuits design. However, as a nano-scale device, the process variation control in the manufacturing of memristors is very difficult. The impact of the process variations on a neural network system that relies on the continuous (analog) states of the memristor could be significant due to the deviation of the memristor state from the designed value. So a complete process variation analysis on memristor is necessary for the application in neural network. Due to the different physical mechanisms, TiO ₂ -based memristor and spintronic memristor demonstrate very different electrical characteristics even when exposing the two types of devices to the same excitations and under the same process variation conditions. In this work, the impact of different geometry variations on the electrical properties of these two different types of memristors was evaluated by conducting the analytic modeling analysis and Monte-Carlo simulations.					
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Statistical memristor model and its applications in neuromorphic computing

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Abstract More than forty years ago, Professor Chua predicted the existence of the memristor to complete the set of passive devices that previously includes only resistor, capacitor, and inductor. However, till 2008 the first physical realization of memristors was demonstrated by HP Lab. The unique properties of memristor create great opportunities in future system design. For instance, the memristor has demonstrated the similar function as synapse, which makes it promising to utilize memristor in neuromorphic circuits design. However, as a nano-scale device, the process variation control in the manufacturing of memristors is very difficult. The impact of the process variations on a neural network system that relies on the continuous (analog) states of the memristor could be significant due to the deviation of the memristor state from the designed value. So a complete process variation analysis on memristor is necessary for the application in neural network. Due to the different physical mechanisms, TiO_2 -based memristor and spintronic memristor demonstrate very different electrical characteristics even when exposing the two types of devices to the same excitations and under the same process variation conditions. In this work, the impact of different geometry variations on the electrical properties of these two different types of memristors was evaluated by conducting the analytic modeling analysis and Monte-Carlo simulations. A simple algorithm, which is based on the latest characterization method of LER (line edge roughness) and thickness fluctuation problems, was proposed to generate a large volume of geometry variation-aware three-dimensional device structures for Monte-Carlo simulations. We investigate the different responses of the static and memristive parameters of the two devices and analyze its implication to the electrical properties of the memristors. Furthermore, a process-variation aware device model can be built based on

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our work. Both corner model and statistical model can be provided depending on users' requirements. Our device models make it possible for scientists and engineers to design neuromorphic circuits with memristive devices, and therefore, to convert virtual neural network in super computer to the real hardware memristive system in the future. Rather than the existing crossbar-based neuron network designs, we focus on memristor-based synapse and the corresponding training circuit to mimic the real biological system. The basic synapse design is presented, and the training sharing scheme and explore design implication on multi-synapse neuron system have been explored.

1 Introduction

In 1971, Professor Leon Chua predicted the existence of the memristor [1]. However, the first physical realization of memristors was demonstrated by HP Lab very recently in 2008, in which the memristive effect was achieved by moving the doping front along a TiO_2 thin-film device [2]. Soon, memristive systems on spintronic devices were proposed [3].

The unique properties of memristors create great opportunities in future system design. For instance, the non-volatility and excellent scalability make it a promising candidate as the next-generation high-performance high-density storage technology [4]. More importantly, memristors have an intrinsic and remarkable feature called a "pinched hysteresis loop" in the $i-v$ plot, that is, memristors can "remember" the total electric charge flowing through them by changing their resistances (memristances) [5]. For example, the applications of this memristive behavior in electronic neural networks have been extensively studied [6][7].

As process technology shrinks down to decananometer (sub-50nm) scale, device parameter fluctuations incurred by process variations have become a critical issue affecting the electrical characteristics of devices [8]. The situation in a memristive system could be even worse when utilizing the analog states of the memristors in design: variations of device parameters, e.g. the instantaneous memristance, can result in the shift of electrical responses, e.g. current. The deviation of the electrical excitations will affect memristance because the total charge through a memristor indeed is the historic behavior of its current profile. Previous works on memristor variation analysis mainly focused on its impacts on non-volatile memory design [4][9]. However, the systematic analysis and quantitative evaluation on how process variations affect the memristive behavior still needs to be done. Our work explores the implications of the device parameters of memristors to the circuit design by taking into account the impact of process variations. The evaluations were conducted based on both theoretical analysis and Monte Carlo simulations.

The device geometry variations significantly influence the electrical properties of nano-devices [10]. For example, the random uncertainties in lithography and patterning processes lead to the random deviation of line edge print-images from their ideal pattern, which is called line edge roughness (LER) [11]. Thickness fluctuation

(TF) is caused by deposition processes in which mounds of atoms form and coarsen over time. As technology shrinks, the geometry variations do not decrease accordingly. In this work, we propose an algorithm to generate a large volume of three-dimensional memristor structures to mimic the geometry variations for Monte-Carlo simulations. The LER model is based on the latest LER characterization method for electron beam lithography (EBL) technology from top-down scanning electron microscope (SEM) measurement [12].

Some previous experimental results showed that the geometry variations are the dominate fluctuation source as process technology further scales down [8]. Therefore, we mainly focus on the impacts of geometry variations in this work. However, other process variations such as random discrete doping (RDD) could also result in the fluctuations of the electrical properties of devices. RDD is an important and complex contributor to the variation in MOSFET and other nano-devices since technology node becomes $90nm$ or less. Statistically, RDD is independent to LER and TF [13][14], the study of RDD on memristor is a good complementary portion to this work. We will explore it in the future work.

Memristive function can be achieved by various materials and device structures. However, the impact of the process variations on the electrical properties of different memristors could be very different even under the same excitations. Therefore, two types of memristors, TiO_2 -based memristor [3] and spintronic memristor [15], are analyzed and evaluated in our work. These two examples are selected because they respectively represent two important mechanisms: solid state and magnetic. However, our proposed modeling methodologies and design philosophies are not limited by the specific types of devices and can be easily extended to the other structures/materials with necessary modifications.

Our contributions can be summarized as follows:

- We investigate the impacts of geometry variations on the electrical properties of memristors and explore their implications to circuit design. Monte Carlo simulations are conducted for quantitative evaluations.
- An algorithm for fast generation of three-dimensional memristor structures is proposed to mimic the geometry variations incurred by EBL technology. The generated samples are used for Monte-Carlo simulations.
- The memristive behavior analysis and evaluations of both TiO_2 -based and spintronic memristors are presented.
- We propose a single memristor-based synapse structure and the corresponding training circuit design that can be used in neuromorphic computing system. The design optimization and its implementation in multi-synapse systems are discussed.

2 Preliminaries

2.1 Memristor Theory

The original definition of the memristor is derived from circuit theory: besides resistor, capacitor and inductor, there must exist the fourth basic two-terminal element that uniquely defines the relationship between the magnetic flux (ϕ) and the electric charge (q) passing through the device [1], or

$$d\phi = M \cdot dq. \quad (1)$$

Considering that magnetic flux and electric charge are the integrals of voltage (V) and current (I) over time, respectively, the definition of the memristor can be generalized as:

$$\begin{cases} V = M(\omega, I) \cdot I \\ \frac{d\omega}{dt} = f(\omega, I) \end{cases} \quad (2)$$

Here, ω is a state variable; $M(\omega, I)$ represents the instantaneous memristance, which varies over time. For a “pure” memristor, neither $M(\omega, I)$ nor $f(\omega, I)$ is an explicit function of I [5].

2.2 Basics of TiO_2 Thin-Film Memristor

In 2008, HP Lab demonstrated the first intentional memristive device by using a Pt/ TiO_2 /Pt thin-film structure [2]. The conceptual view is illustrated in Fig. 1(a): two metal wires on Pt are used as the top and bottom electrodes, and a thick titanium dioxide film is sandwiched in between. The stoichiometric TiO_2 with an exact 2:1 ratio of oxygen to titanium has a natural state as an insulator. However, if the titanium dioxide is lacking a small amount of oxygen, its conductivity becomes relatively high like a semiconductor. We call it oxygen-deficient titanium dioxide (TiO_{2-x}) [9]. The memristive function can be achieved by moving the doping front:

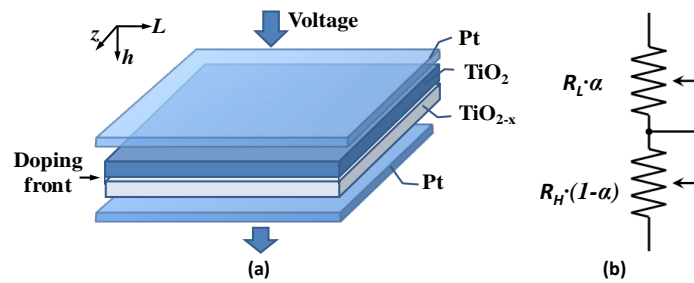


Fig. 1 TiO_2 thin-film memristor. (a) structure, and (b) equivalent circuit.

A positive voltage applied on the top electrode can drive the oxygen vacancies into the pure TiO_2 part and therefore lower the resistance continuously. On the other hand, a negative voltage applied on the top electrode can push the dopants back to the TiO_{2-x} part and hence increase the overall resistance. For a TiO_2 -based memristor, R_L (R_H) is used to denote the lowest (highest) resistance of the structure.

Fig. 1(b) illustrates a coupled variable resistor model for a TiO_2 -based memristor, which is equivalent to two series-connected resistors. The overall resistance can be expressed as

$$M(\alpha) = R_L \cdot \alpha + R_H \cdot (1 - \alpha). \quad (3)$$

Here α ($0 \leq \alpha \leq 1$) is the relative doping front position, which is the ratio of doping front position over the total thickness of TiO_2 thin-film.

The velocity of doping front movement $v(t)$, which is driven by the voltage applied across the memristor $V(t)$ can be expressed as

$$\frac{v(t)}{h} = \frac{d\alpha}{dt} = \mu_v \cdot \frac{R_L}{h^2} \cdot \frac{V(t)}{M(\alpha)} \quad (4)$$

where, μ_v is the equivalent mobility of dopants, h is the total thickness of the TiO_2 thin-film; and $M(\alpha)$ is the total memristance when the relative doping front position is α .

Filamentary conduction has been observed in nano-scale semiconductors, such as TiO_2 . It shows that the current travels through some high conducting filaments rather than passes the device evenly [17][18]. However, there is no device model based on filamentary conduction mechanism yet. Considering that the main focus of this work is the process variation analysis method of the memristor, which can be separated from the explicit physical model of memristor, the popular bulk model of TiO_2 is applied. We will extend the research by integrating the device model based on filamentary conduction in our future work.

Recent experiments showed that μ_v is not a constant but grows exponentially when the bias voltage goes beyond certain threshold voltage [19]. Nevertheless, the structure of TiO_2 memristor model, *i.e.*, Eq. (3), still remains valid.

2.3 Basics of Spintronic Memristor

Among all the spintronic memristive devices, the one based on magnetic tunneling junction (MTJ) could be the most promising one because of its simple structure [3][15]. The basic structure of magnetic memristor could be either giant magneto-resistance (GMR) or tunneling magneto-resistance (TMR) MTJs. We choose TMR-based structure shown in Fig. 2(a) as the objective of this work because it has a bigger difference between the upper and the lower bounds of total memristance (resistance).

There have been many research activities investigated on the spintronic memristor or the similar device structure, such as the racetrack structure proposed by

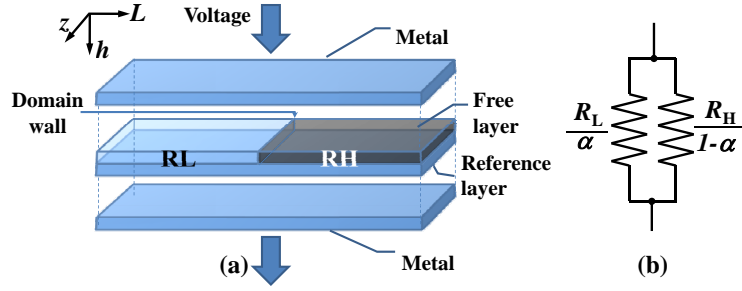


Fig. 2 TMR-based spintronic memristor. (a) structure, and (b) equivalent circuit.

IBM [20]. Very recently, NEC Lab reported the free layer switching through the domain wall movement [21], which indeed is a spintronic memristor.

An MTJ is composed of two ferromagnetic layers and an oxide barrier layer, e.g. MgO. The bottom ferromagnetic layer is called reference layer, of which the magnetization direction is fixed by coupling to a pinned magnetic layer. The top ferromagnetic layer called free layer is divided into two magnetic domains by a domain-wall: the magnetization direction of one domain is parallel to the reference layer's, while the magnetization direction of the other domain is anti-parallel to the reference layer's.

The movement of the domain wall is driven by the spin-polarized current, which passes through the two ferromagnetic layers. For example, applying a positive voltage on free layer can impel the domain wall to increase the length of the magnetic domain with a magnetization direction parallel to the reference layer's and hence reduce the MTJ resistance. On the other hand, applying a positive voltage on reference layer will reduce the length of the magnetic domain with a magnetization direction parallel to the reference layer's. Therefore, the MTJ resistance increases. If the width of the domain with the magnetization direction anti-parallel (parallel) to the reference layer's is compressed to close to zero, the memristor has the lowest (highest) resistance, denoted as R_L (R_H).

As shown in Fig. 2(b), the overall resistance of a TMR-base spintronic memristor can be modeled as two parallel connected resistors with resistances R_L / α and $R_H / (1 - \alpha)$, respectively [15]. This structure has also been experimentally proved [22]. Here α ($0 \leq \alpha \leq 1$) represents the relative domain wall position as the ratio of the domain wall position (x) over the total length of the free layer (L). The overall memristance can be expressed as

$$M(\alpha) = \frac{R_L \cdot R_H}{R_H \cdot \alpha + R_L(1 - \alpha)}. \quad (5)$$

How fast the domain-wall can move is mainly determined by the strength of spin-polarized current. More precisely, the domain-wall velocity $v(t)$ is proportional to the current density J [23]. We have

$$J(t) = \frac{V(t)}{M(\alpha) \cdot L \cdot z}, \quad (6)$$

and

$$v(t) = \frac{d\alpha(t)}{dt} = \frac{\Gamma_v}{L} \cdot J_{eff}(t), J_{eff} = \begin{cases} J, J \geq J_{cr} \\ 0, J \leq J_{cr}. \end{cases} \quad (7)$$

Here Γ_v is the domain wall velocity coefficient, which is related to device structure and material property. L and z are the total length and width of the spintronic memristor, respectively. The domain wall movement in the spintronic memristor happens only when the applied current density (J) is above the critical current density (J_{cr}) [23][24][25][26][27].

3 Mathematical Analysis

The actual length (L) and width (z) of a memristor is affected by LER. The variation of thickness (h) of a thin film structure is usually described by TF. As a matter of convenience, we define that, the impact of process variations on any given variable can be expressed as a factor $\theta = \frac{\omega'}{\omega}$, where ω is its ideal value, and ω' is the actual value under process variations.

The ideal geometry dimensions of the TiO_2 thin-film memristor and spintronic memristor used in this work are summarized in Table 1.

3.1 TiO_2 Thin-Film Memristor

In TiO_2 thin-film memristors, the current passes through the device along the thickness (h) direction. Ideally the doping front has an area $S = L \cdot z$. To simulate the impact of LER on the electrical properties, the memristor device is divided into many small filaments between the two electrodes. Each filament i has a cross-section area ds and a thickness h . Fig. 3 demonstrates a non-ideal 3D structure of a TiO_2 memristor (i.e., with geometry variations in consideration), which is partitioned into many filaments in statistical analysis.

As shown in Fig. 3, ideally, the cross-section area of a filament is ds/S of the entire device area and its thickness is h . Thus, for filament i , the ideal upper bound and lower bound of the memristance can be expressed as

Table 1 The device dimensions of memristors.

	Length(L)	Width(z)	Thickness(h)
Thin-film	50 nm	50 nm	10 nm
Spintronic	200 nm	10 nm	7 nm

$$R_{i,H} = R_H \cdot \frac{S}{ds}, \text{ and } R_{i,L} = R_L \cdot \frac{S}{ds}. \quad (8)$$

Here, $\theta_{i,s}$ represents the variation ratio on the cross-section area ds , which is caused by 2-D LER. Similarly, $\theta_{i,h}$ is the variation ratio on thickness h due to TF. The resistance of a filament is determined by its section area and thickness, *i.e.*, $R = \rho \cdot \frac{h}{s}$, where ρ is the resistance density. Therefore, the actual upper and the lower bound under the process variations can be expressed as

$$R'_{i,H} = R_{i,H} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}, \text{ and } R'_{i,L} = R_{i,L} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}. \quad (9)$$

If a filament is small enough, we can assume it has a flat doping front. Then, the actual doping front velocity in filament i considering process variations can be calculated by replacing the ideal values with actual values in Eq.(4). We have

$$v'_i(t) = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{M'_i(\alpha'_i)}. \quad (10)$$

Here h' and M'_i are the actual thickness and memristance of filament i . Then, we can get a set of related equations for filament i , including the doping front position

$$\alpha'_i(t) = \int_0^t v'(\tau) \cdot d\tau, \quad (11)$$

the corresponding memristance

$$M'_i(\alpha'_i) = \alpha'_i \cdot R'_{i,L} + (1 - \alpha'_i) \cdot R'_{i,H}, \quad (12)$$

and the current through the filament i

$$I'_i(t) = \frac{V(t)}{M'_i(\alpha'_i)}. \quad (13)$$

By combining Eq. (10) – (13), the doping front position in every filament i under process variations $\alpha'_i(t)$ can be obtained by solving the differential equation

$$\frac{d\alpha'_i(t)}{dt} = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{\alpha'_i(t) \cdot R'_{i,L} + (1 - \alpha'_i(t)) \cdot R'_{i,H}}. \quad (14)$$

Eq. (14) indicates that the behavior of the doping front movement is dependent on the specific electrical excitations, *e.g.*, $V(t)$.

For instance, applying a sinusoidal voltage source to the TiO_2 thin-film memristor such as

$$V(t) = V_m \cdot \sin(2\pi f \cdot t), \quad (15)$$

the corresponding doping front position of filament i can be expressed as:

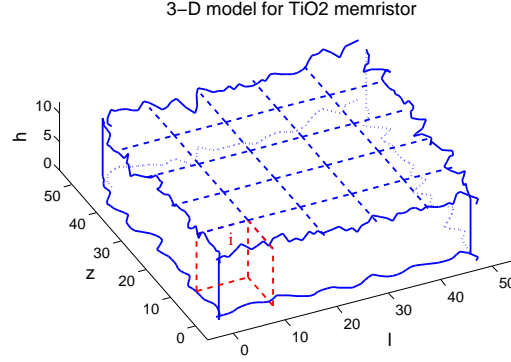


Fig. 3 An example of 3D TiO₂ memristor structure, which is partitioned into many filaments in statistical analysis.

$$\alpha'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 - A \cdot B(t) \cdot \frac{2}{\theta_{i,h}^2} + 2C \cdot A \cdot \frac{\theta_{i,s}}{\theta_{i,h}}}}{A}. \quad (16)$$

Where, $A = R_{i,H} - R_{i,L}$, $B(t) = \mu_v \cdot R_{i,L} \cdot V_m \cdot \cos(2\pi f \cdot t)$, and C is an initial state constant.

The term $B(t)$ accounts for the effect of electrical excitation on doping front position. The terms $\theta_{i,s}$ and $\theta_{i,h}$ represent the effect of both LER and TF on memristive behavior. Moreover, the impact of the geometry variations on the electrical properties of memristors could be affected by the electrical excitations. For example, we can set $\alpha(0) = 0$ to represent the case that the TiO₂ memristor starts from $M(0) = R_H$. In such a condition, C becomes 0, and hence, the doping front position $\alpha'_i(t)$ can be calculated as:

$$\alpha'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 - A \cdot B(t) \cdot \frac{2}{\theta_{i,h}^2}}}{A}, \quad (17)$$

which is affected only by TF and electrical excitations. LER will not disturb $\alpha'_i(t)$ if the TiO₂ thin-film memristor has an initial state $\alpha(0) = 0$.

The overall memristance of the memristor can be calculated as the total resistance of all n filaments connected in parallel. Again, i denotes the i^{th} filament. When n goes to ∞ , we can have

$$R'_H = \frac{1}{\int_0^\infty 1/R'_{i,H} \cdot di} = R_H \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s} \cdot di}, \quad (18)$$

and

$$R'_L = \frac{1}{\int_0^\infty 1/R'_{i,L} \cdot di} = R_L \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s} \cdot di}. \quad (19)$$

The overall current through the memristor is the sum of the current through each filament:

$$I'(t) = \int_0^\infty I'_i(t) \cdot di. \quad (20)$$

The instantaneous memristance of the overall memristor can be defined as

$$M'(t) = \frac{V(t)}{I'(t)} = \frac{1}{\int_0^\infty 1/M'_i \cdot di}. \quad (21)$$

Since the doping front position movement in each filament will not be the same because h'_i varies due to TF (and/or the roughness of the electrode contact), we define the average doping front position of the whole memristor as:

$$\alpha'(t) = \frac{R'_H - M'(t)}{R'_H - R'_L}. \quad (22)$$

3.2 Spintronic Memristor

Since the length of a spintronic memristor is usually much longer than the other two dimensions, the impact of the variance in length on the spintronic memristor's electrical properties can be ignored. In our analysis, the device can be chopped into infinite segments along the length direction as shown in Fig. 4. For a segment i , the upper and lower bounds of memristance are:

$$R'_{i,H} = R_{i,H} \cdot \frac{\theta_{i,h}}{\theta_{i,z}}, \text{ and } R'_{i,L} = R_{i,L} \cdot \frac{\theta_{i,h}}{\theta_{i,z}}. \quad (23)$$

Here we assume the ideal memristance changes linearly within the domain wall, or M_i changes linearly from $R_{j,L}$ to $R_{k,H}$ when $j < i < k$. Here j and k are the

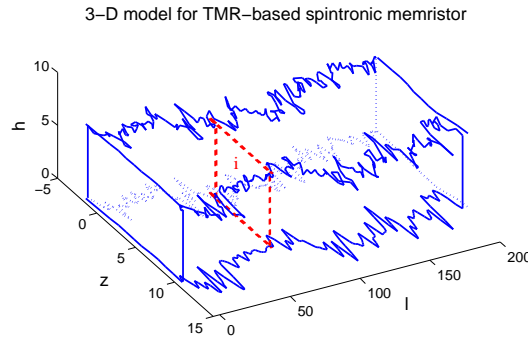


Fig. 4 An example of 3D TMR-based spintronic memristor structure, which is partitioned into many filaments in statistical analysis.

two segments at the two boundaries of domain wall and connected to the magnetic domains with either the low or the high resistance states. The memristance of each segment is

$$M'_i = \begin{cases} R'_{i,L}, & i < \alpha' \\ R'_{i,H}, & i \geq \alpha' \end{cases} \quad (24)$$

So for overall resistance R'_H and R'_L , we have

$$R'_H = \frac{1}{\int_0^\infty 1/R'_{i,H} \cdot di} = R_H \cdot \frac{1}{\int_0^\infty \theta_{i,z}/\theta_{i,h} \cdot di}, \quad (25)$$

and

$$R'_L = \frac{1}{\int_0^\infty 1/R'_{i,L} \cdot di} = R_L \cdot \frac{1}{\int_0^\infty \theta_{i,z}/\theta_{i,h} \cdot di}. \quad (26)$$

Then the memristance of the whole device is

$$\begin{aligned} M'(\alpha') &= \frac{1}{\int_0^{\alpha'} \frac{1}{R'_{i,L}} di + \int_{\alpha'}^1 \frac{1}{R'_{i,H}} di} \\ &= \frac{1}{\int_0^{\alpha'} \frac{1}{R_{i,L}} \cdot \frac{\theta_{i,z}}{\theta_{i,h}} di + \int_{\alpha'}^1 \frac{1}{R_{i,H}} \cdot \frac{\theta_{i,z}}{\theta_{i,h}} di} \end{aligned} \quad (27)$$

Here the width of each segments z_i varies segment by segment due to the LER effect. The statistical behavior of spintronic memristors can still be evaluated by Monte-Carlo simulation in Section 5.

We assume the current density applied on the domain wall $J'(t)$ is the one of the segments i where the domain wall located in the middle:

$$J'(t) = J'_i = \frac{V(t)}{M'(\alpha') \cdot L \cdot z'_i}. \quad (28)$$

Then the domain wall velocity under process variations can be calculated as:

$$\begin{aligned} v'(t) = v'_i &= \frac{d\alpha'(t)}{dt} = \frac{\Gamma_v}{L} \cdot J'_{eff}(t), \\ J'_{eff} &= \begin{cases} J', & J' \geq J_{cr} \\ 0, & J' < J_{cr} \end{cases} \end{aligned} \quad (29)$$

4 3D Memristor Structure Modeling

Analytic modeling is a fast way to estimation the impact of process variations on memristors. However, we noticed that in modeling some variations analytically, e.g. simulating the LER, may be beyond the capability of analytic model [12]. The data

on silicon variations, however, is usually very hard to obtain simply due to intellectual property protection. To improve the accuracy of our evaluations, we create a simulation flow to generate 3-D memristor samples with the geometry variations including LER and thickness fluctuation. The correlation between the generated samples and the real silicon data are guaranteed by the sanity check of the LER characterization parameters. The flow is shown in Fig. 5.

Many factors affecting the quality of the line edges show different random effects. Usually statistical parameters such as the auto-correlation function (ACF) and power spectral density (PSD) are used to describe the property of the line edges.

ACF is a basic statistical function of the wavelength of the line profile, representing the correlation of point fluctuations on the line edge at different position. PSD describes the waveform in the frequency domain, reflecting the ratio of signals with different frequencies to the whole signal.

Considering that LER issues are related to fabrication processes, we mainly target the nano-scale pattern fabricated by electron beam lithography (EBL). The measurements show that under such a condition, the line edge profile has two important properties: (1) the line edge profile in ACF figure demonstrates regular oscillations, which are caused by periodic composition in the EBL fabrication system; and (2) the line edge roughness mainly concentrates in a low frequency zone, which is reflected by PSD figure [12].

To generate line edge samples close to the real cases, we can equally divide the entire line edge into many segments, say, n segments. Without losing the LER properties in EBL process, we modified the random LER modeling proposed in [28] to a simpler form with less parameters. The LER of the i^{th} segment can be modeled by

$$LER_i = L_{LF} \cdot \sin(f_{max} \cdot x_i) + L_{HF} \cdot p_i. \quad (30)$$

The first term on the right side of Eq. (30) represents the regular disturbance at the low frequency range, which is modeled as a sinusoid function with amplitude L_{LF} . f_{max} the mean of the low frequency range derived from PSD analysis. Without

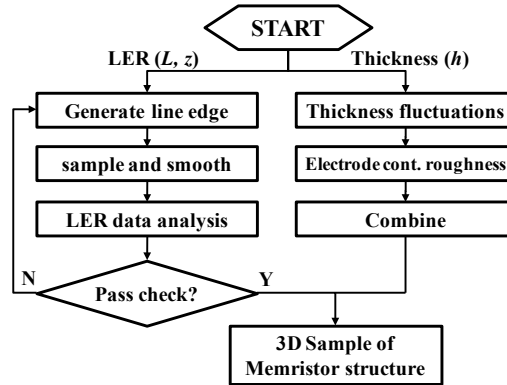


Fig. 5 The flow of 3D memristor structure generation including geometry variations.

Table 2 The parameters/constraints in LER characterization.

Parameters		Constraints	
L_{LF}	0.8 nm	σ_{LER}	2.5nm \sim 3.5nm
f_{max}	1.8 MHz	σ_{LWR}	4.0nm \sim 5.0nm
L_{HF}	0.4 nm	Sk	0.1nm \sim 0.2nm
$/$	$/$	Ku	2.5nm \sim 3.5nm

loss of generality, a uniform distribution $x_i \in U(-1, 1)$ is used to represent an equal distribution of all frequency components in the low frequency range. The high frequency disturbances are also taken into account by the second term on the right side of Eq. (30) as a Gaussian white noise with amplitude L_{HF} . Here p_i follows the normal distribution $N(0, 1)$ [12]. The actual values of L_{LF} , L_{HF} and f_{max} are determined by ACF and PSD.

To ensure the correlation between the generated line edge samples with the measurement results, we introduce four constraints to conduct a sanity check of the generated samples:

- σ_{LER} : the root mean square (RMS) of LER;
- σ_{LWR} : the RMS of line width roughness (LWR);
- Sk : skewness, used to specify the symmetry of the amplitude of the line edge; and
- Ku : kurtosis, used to describe the steepness of the amplitude distribution curve.

The above four parameters are widely used in LER characterization and can be obtained from measurement results directly [12]. Only the line edge samples that satisfy the constraints will be taken as valid device samples. Table 2 summarizes the parameters used in our algorithm, which are correlated with the characterization method and experimental results in [12]. And Fig. 6 shows the LER characteristic parameters distribution among 1000 Monte-Carlo simulations.

Even the main function has captured the major features of LER, it is not enough to mimic all the LER characteristics. The difference between real LER distribution and our modeling function results in the fact that some generated samples are not qualified compared to the characteristic parameters, or the constraints of the real LER profile. Thus, sanity check which screens out the unsuccessful results is necessary. Only those samples in red rectangles shown in Fig. 6 satisfy the constraints and will be used for the device electrical property analysis. The criteria of the sanity check are defined based on the measurement results of real LER data.

The thickness fluctuation is caused by the random uncertainties in sputter deposition or atomic layer deposition. It has a relatively smaller impact than the LER and can be modeled as a Gaussian distribution. Since the memristors in this work have relatively bigger dimensions in the horizontal plane than the thickness direction (shown in Table 1), we also considered roughness of electrode contact in our simulation: The means of the thickness of each memristor is generated by assuming it follows the Gaussian distribution. Each memristor is then divided into many filaments between the two electrodes. The roughness of electrode contacts is modeled

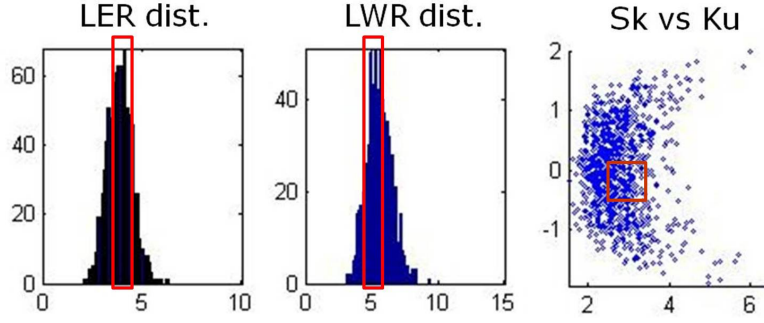


Fig. 6 LER characteristic parameters distribution among 1000 Monte-Carlo simulations. Constraints are shown in red rectangles.

based on the variations of the thickness of each filament. Here, we assume that both thickness fluctuations and electrode contact roughness follow Gaussian distributions with a deviation $\sigma = 2\%$ of thin film thickness.

Fig. 3 is an example of 3D structure of a TiO_2 thin-film memristor generated by the proposed flow. It illustrates the effects of all the geometry variations on a TiO_2 memristor device structure. According to Section 3, a 2-D partition is required for the statistical analysis. In the given example, we partition the device into 25 small filaments with the ideal dimensions of $L = 10\text{nm}$, $z = 10\text{nm}$, and $h = 10\text{nm}$. Each filament can be regarded as a small memristor, which is affected by either only TF or both LER and TF. The overall performance of device can be approximated by paralleled connecting all the filaments.

Similarly, Fig. 4 is an example of 3D structure of a TMR-based spintronic memristor. Since the length of a spintronic memristor is much longer than its width and height, only 1-D partition along the length direction is required. In this case, the device is divided into 200 filaments. Ideally, each filament has $L = 1\text{nm}$, $z = 10\text{nm}$, and $h = 7\text{nm}$. Each filament i is either in the low resistance state $R'_{i,L}$ or the high resistance state $R'_{i,H}$, with considering the effects of both LER and TF. The overall performance of device can be approximated by paralleled connecting all the filaments.

5 Experimental Results

5.1 Simulation Setup

To evaluate the impact of process variations on the electrical properties of memristors, we conducted Monte-Carlo simulations with 10,000 qualified 3-D device samples generated by our proposed flow. A sinusoidal voltage source shown in Eq.

Table 3 Memristor Devices and electrical parameters

TiO ₂ thin-film memristor [2]					
$R_L(\Omega)$	$R_H(\Omega)$	$\mu_v(\text{m}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1})$	/	$V_m(\text{V})$	$f(\text{Hz})$
100	16000	10^{-14}	/	1	0.5
Spintronic memristor [15]					
$R_L(\Omega)$	$R_H(\Omega)$	$\Gamma_v(\text{nm}^3 \cdot \text{C}^{-1})$	$J_{cr}(\text{A} / \text{nm}^2)$	$V_m(\text{V})$	$f(\text{Hz})$
2500	7500	2.01×10^{-14}	2.00×10^{-8}	2	10M

(15) is applied as the external excitation. The initial state of the memristor is set as $M(\alpha = 0) = R_H$. The device and electrical parameters used in our simulations are summarized in Table 3. Both separate and combined effects of geometry variations on various properties of memristors are analyzed, including:

- the distribution of R_H and R_L ;
- the change of memristance $M(t)$ and $M(\alpha)$;
- the velocity of wall movement $v(\alpha)$;
- the current through memristor $i(t)$; and
- the I-V characteristics.

5.2 TiO₂ Thin-Film Memristor

The $\pm 3\sigma$ (minimal/maximal) values of the device/electrical parameters as the percentage of the corresponding ideal values are summarized in Table 4. For those parameters that vary over time, we consider the variation at each time step of all the

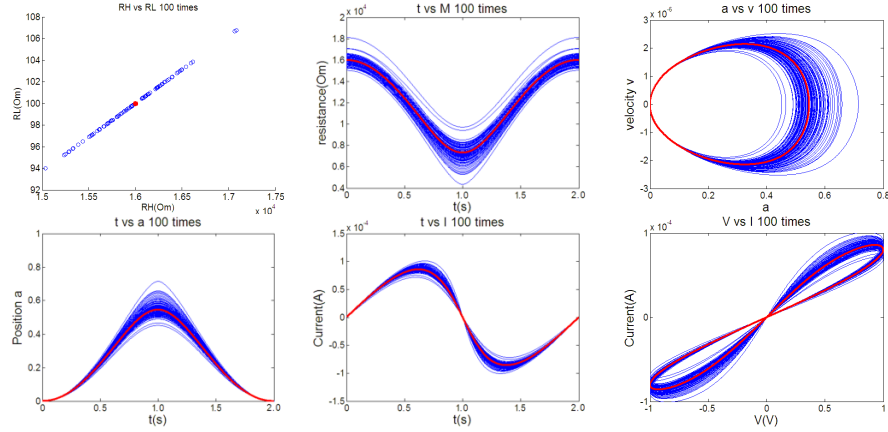


Fig. 7 Simulation results for TiO₂ thin-film memristors. The blue curves are from 100 Monte-Carlo simulations, and red lines are the ideal condition. From top left to right bottom, the figures are R_H vs. R_L ; $M(t)$ vs. t ; v vs. α ; α vs. t ; I vs. t ; and $I - V$ characteristics.

Table 4 3σ min./max. of TiO_2 memristor parameters

Sinusoidal Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-5.4	4.1	-5.5	4.8	-6.4	7.3
$M(\alpha)$	-5.4	4.1	-37.1	20.8	-36.5	24.1
$\alpha(t)$	0.0	0.0	-13.3	27.5	-14.7	27.4
$v(\alpha)$	0.0	0.0	-9.3	15.6	-10.4	16.9
$i(\alpha)$	-4.7	5.7	-9.3	15.7	-10.7	17.2
Power	-4.7	5.7	-8.8	14.1	-10.1	15.6

Square wave Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-5.3	3.7	-6.2	5.2	-6.6	6.9
$M(\alpha)$	-5.3	3.7	-17.8	13.2	-15.4	14.4
$\alpha(t)$	0.0	0.0	-12.1	16.6	-13.0	15.6
$v(\alpha)$	0.0	0.0	-11.6	17.7	-12.5	16.7
$i(\alpha)$	-4.0	5.2	-11.7	17.7	-12.6	17.6
Power	-4.0	5.2	-7.7	9.8	-8.5	10.1

devices. The simulation results considering only either LER or TF are also listed. To visually demonstrate the overall impact of process variations on the memristive behavior of TiO_2 memristors, the dynamic responses of 100 Monte Carlo simulations are shown in Fig. 7.

Table 4 shows that the static behavior parameters of memristors, i.e., R_H and R_L , are affected in a similar way by both LER and thickness fluctuations. This is consistent to our analytical results in Eq. (18) and (19), which show that θ_s and θ_h have the similar effects on the variation of R'_H and R'_L .

However, thickness fluctuation shows a much more significant impact on the memristive behaviors such as $v(t)$, $\alpha(t)$ and $M(\alpha)$, than LER does. It is because the doping front movement is along the thickness direction: $v(t)$ is inversely proportional to the square of the thickness, and $\alpha(t)$ is the integral of $v(t)$ over time as shown in Eq. (10) and (11). For the same reason, thickness fluctuations significantly affect the instantaneous memristance $M(\alpha)$ as well.

Because the thickness of the TiO_2 memristor is relative small compared to other dimensions, we assume the doping front cross-section area is a constant along the thickness direction in our simulation. The impact of LER on $\alpha(t)$ or $v(t)$, which is relatively small compared to that of the thickness fluctuations, is ignored in Table 4.

An interesting observation in Fig. 7 is that as the doping front α moves toward 1, the velocity v regularly grows larger and reaches its peak at the half period of the sinusoidal excitation, i.e. $t=1\text{s}$. This can be explained by Eq. (12): the memristance is getting smaller as α moves toward 1. With the same input amplitude, a smaller resistance will result in a bigger current and therefore a bigger variation on $v(t)$. Similarly, memristance $M(\alpha)$ reaches its peak variance when α is close to 1.

We also conduct $10,000 \times$ Monte Carlo simulations on the same samples by applying a square wave voltage excitation. The amplitude of the voltage excitation is $\pm 0.5\text{V}$. The simulation results are also shown in Table 4. The results of the static

behavior parameters, i.e., R_H and R_L , are exactly the same as those with sinusoidal voltage inputs because they are independent of the external excitations, The results of the memristive behavior parameters such as $v(t)$, $\alpha(t)$ and $M(\alpha)$ show similar trends as those with the sinusoidal voltage inputs. Based on Eq. (16), $\alpha(t)$'s variance is sensitive to the type and amplitude of electrical excitation, because $B(t)$ greatly affects the weight of the thickness fluctuation parameter. That is why the thickness fluctuation has a significantly impact on the electrical properties of memristors under sinusoidal and square voltage excitations.

5.3 Spintronic Memristor

The $\pm 3\sigma$ values of the device/electrical parameters based on 10,000 Monte-Carlo simulations are summarized in Table 5. The visual demonstration of 100 Monte-Carlo simulations with a sinusoidal voltage excitation is shown in Fig. 8.

For the spintronic memristor, the impact of LER on the electrical properties of memristors is more than that of thickness fluctuation. This is because the direction of the domain wall movement is perpendicular to the direction of spin-polarized current. The impact of thickness fluctuations on very small segments cancel each other during the integral along the direction of the domain wall movement.

"LER only" simulation results show that the $+3\sigma$ corner of LER has more impact on the electrical properties than that of -3σ corner. This is because the line width variation is the dominant factor on the variation of electrical properties of spintronic memristors, and the line edge profiles used in our LER parameters have

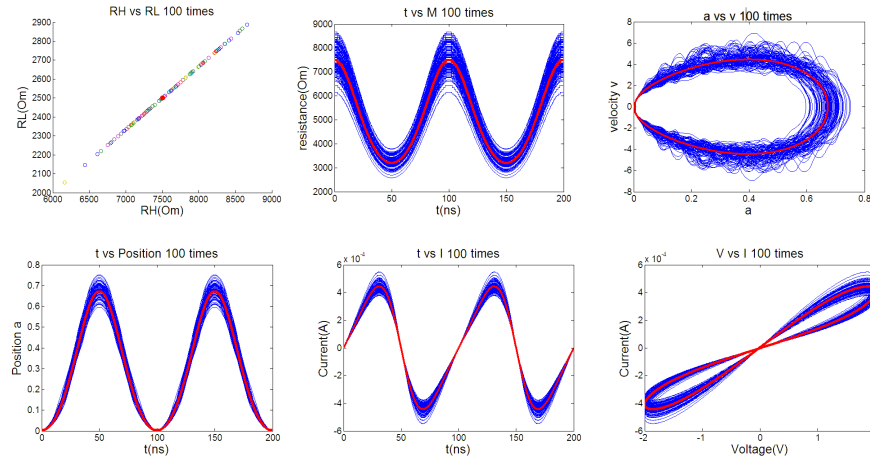


Fig. 8 Simulation results for spintronic memristors. The blue curves are from 100 Monte-Carlo simulations, and red lines are the ideal condition. From top left to right bottom, the figures are R_H vs. R_L ; $M(t)$ vs. t ; v vs. α ; α vs. t ; I vs. t ; and $I - V$ characteristics.

Table 5 3σ min./max. of spintronic memristor parameters

Sinusoidal Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-15.3	22.9	-6.1	5.8	-16.4	20.9
$M(\alpha)$	-15.1	23.3	-11.0	11.0	-16.3	21.1
$\alpha(t)$	-9.7	8.1	-8.4	9.5	-11.8	8.1
$v(\alpha)$	-10.7	22.1	-9.1	9.9	-21.5	22.5
$i(\alpha)$	-18.5	18.5	-8.9	10.1	-17.7	17.8
Power	-18.4	18.6	-8.3	9.4	-17.8	17.8

Square wave Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-15.8	22.0	-5.3	5.7	-15.9	24.2
$M(\alpha)$	-15.6	21.8	-8.5	9.7	-17.0	25.5
$\alpha(t)$	-13.1	13.8	-7.5	7.7	-17.2	16.2
$v(\alpha)$	-16.5	20.7	-10.0	8.3	-20.1	25.2
$i(\alpha)$	-19.5	17.1	-9.0	9.3	-22.1	20.5
Power	-19.4	17.1	-7.6	7.7	-20.9	19.6

a right-biased feature [12]. Since normal distribution is assumed for the variations of thickness, σ_h has approximately symmetric impact on $\pm 3\sigma$ corners.

The impact of LER on the memristive parameters $v(t)$, $\alpha(t)$ and $M(\alpha)$ is also larger than thickness variation. Again, the impact of thickness fluctuations on very small segments cancel each other during the integral along the direction of the domain wall movement.

Similarly, we also conduct Monte Carlo simulations by applying a square wave voltage excitation. The amplitude of the voltage excitation is $\pm 1V$. The similar trends as that of sinusoidal excitations are observed.

6 Memristor-based Synapse Design

6.1 The Principle of Memristor-based Synapse

Rather than using memristor crossbar array in neuromorphic reconfigurable architecture, we propose a memristor-based synapse design to mimic the biological structure. Fig. 9(a) depicts the conceptual scheme, which simply consists of a NMOS transistor (Q) and a memristor. When the input V_{in} is low, Q is turned off and the output V_{out} is connected to ground through the memristor. On the contrary, when V_{in} is high and turns on Q , memristance M and the equivalent resistance of Q (R_Q) together determine V_{out} :

$$V_{out} = f(V_{in} \cdot M). \quad (31)$$

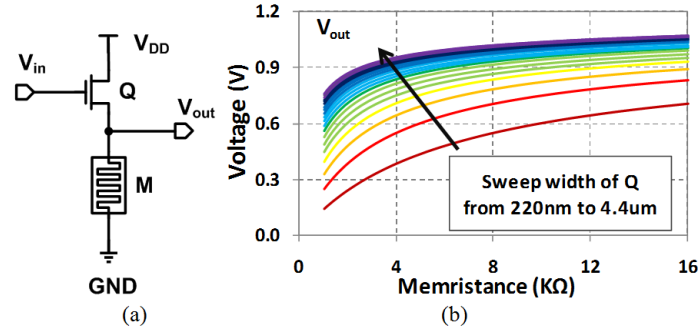


Fig. 9 (a) Proposed synapse design. (b) Synapse output vs. memristance.

Here, V_{out} is weighted by the memristance, which behaves like a synapse. Fig. 9(b) shows the simulated V_{out} when sweeping the memristance from $1K\Omega$ to $16K\Omega$. Here, CMOS devices used TSMC $0.18\mu m$ technology.

Note that the response of the synapse design is dependent on the equivalent resistance of the transistor Q (R_Q), or, the size of Q . This can also be demonstrated in Fig. 9(b) by sweeping the width of Q from $220nm$ to $4.4\mu m$ with a step of $220nm$. The simulation shows that a larger Q can result in a wider range of V_{out} with poorer linearity. However, for a large Q , the enhancement of V_{out} by further increasing its size is marginal. To improve design stability, a buffer can be added at output of the synapse to increase voltage swing. Furthermore, some circuit optimization techniques, such as asymmetry gate in other blocks, can be used to minimize the overall synapse-based system.

6.2 Synapse Training Circuit

Being self-adaptive to the environment is one of the most important properties of a biological synapse. To accomplish the similar functionality, a training block is needed in the memristor-based synapse that can adjust its memristance.

6.2.1 Memristor Training Circuit

Fig. 10(a) shows the diagram of training circuit for one synapse design, based on logic analysis and simplification. It includes two major components: training controller and write driver. By comparing the current synapse output V_{out} and the expected output D_{train} , training controller generates the control signals. The write driver uses these signals to control two pairs of NMOS and PMOS switches and supply training voltage pair V_{top} and V_{bot} . The training pair is applied to the two terminals of the memristor in the synapse design.

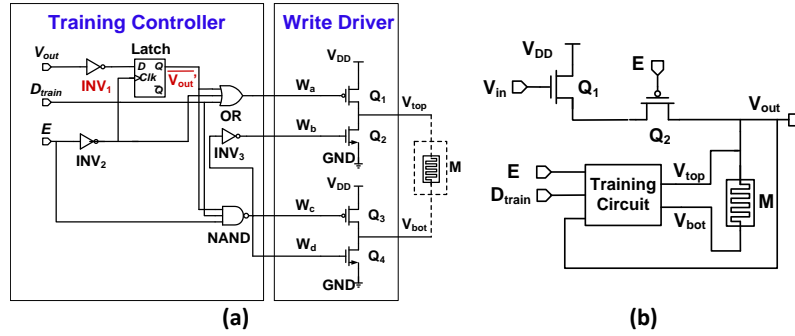


Fig. 10 (a) The training circuit diagram. (b) The proposed synapse together with training circuit.

Determined by the training enable signal E , the training circuit can work under two modes.

- Operating mode: When $E = 0$, the synapse is under regular operating (read) mode, and the training circuit is disabled.
- Training mode: The training circuit is enabled when $E = 1$. By comparing the current synapse output V_{out} and the expected D_{train} , the training circuit generates V_{top} and V_{bot} applied to the two terminals of memristor to update or keep its memristance. We define $V_{mem} = V_{top} - V_{bot}$.

Fig. 10(b) depicts the proposed memristor-based synapse integrated with training circuit. An extra NMOS transistor Q_2 is inserted in synapse to isolate training operation from other voltage sources: when $E = 1$, Q_2 is turned off so that the two terminals of memristor are controlled only by the training circuit, not affected by V_{in} .

The timing diagram of training circuit is demonstrated Fig. 11(a). Before a training procedure starts, a sensing step is required to detect the current V_{out} to be compared with D_{train} . In the sensing phase, accordingly, training enable signal E is set to low for a very short period of time (e.g., 4.5ns) at the beginning of training. At

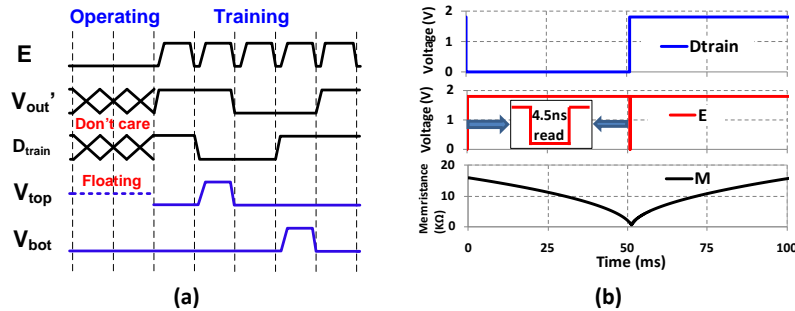


Fig. 11 (a) The timing diagram of training circuit. (b) The simulation result of memristor training.

Table 6 Sizing of INV_1 and Q_1

P/N Ratio	PMOS/NMOS in INV_1	Q_1
2	720nm/360nm	$18 \times 220nm$
2	440nm/220nm	$16 \times 220nm$
1	360nm/360nm	$12 \times 220nm$
1	220nm/220nm	$11 \times 220nm$
0.5	360nm/720nm	$9 \times 220nm$
0.5	220nm/440nm	$9 \times 220nm$

the same time, (V'_{out}) is sent to Latch, whose output (V'_{out}) remains constant during one training period, as shown in Fig. 10(a). In the training phase, E is set back to high for a much longer time (i.e., 51ms) to change the memristance if needed.

We tested the training procedure by using the TiO_2 memristor model [2]. The training circuit was designed by using TSMC 0.18 μm technology with $V_{DD} = 1.8V$. Changing memristance from R_H to R_L or vice versa takes about 51ms. The simulation result is shown in Fig. 11(b). Here, the memristance is initialized as $M = 16K\Omega$. In the first 51ms, it is trained to $1K\Omega$ by setting D_{train} to low. Then at $t = 51ms$, we set D_{train} to high and train the memristance back to R_H in the following 51ms.

6.2.2 Asymmetry Gate Design

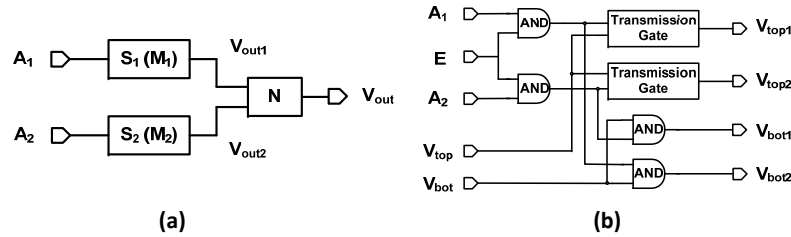


Fig. 12 (a) Two-input neuron structure. (b) Training sharing distribution circuit.

Table 7 Training sharing circuit operation

Status	V_{top1}	V_{bot1}	V_{top2}	V_{bot2}
Training M_1	V_{top}	V_{bot}	Floating	0
Training M_2	Floating	0	V_{top}	V_{bot}

Table 8 Synapse input pairs for different logics

Function of N	Training M_1	Training M_2
OR/NOR	$A_1 = 1, A_2 = 0$	$A_1 = 0, A_2 = 1$
XOR/XNOR	$A_1 = 1, A_2 = 0$	$A_1 = 0, A_2 = 1$
AND/NAND	$A_1 = 1, A_2 = 1$	$A_1 = 1, A_2 = 1$

6.2.3 Multi-synapse Training Scheme

Most of the neuron systems are constructed by multiple synapses. In this subsection, we discuss the corresponding training scheme by taking a 2-synapse neuron in Fig. 12(a) as the example. Here, A_1 and A_2 are two synapse inputs received from other neurons. M_1 and M_2 are memristor-based weights for two synapses S_1 and S_2 . N is denoted for neuron with output V_{out} . The value of V_{out} depends on the functionality of N as well as V_{out1} and V_{out2} from the two synapses. With the different combinations of M_1 and M_2 , the two-input neuron could obtain different functionality.

To save design cost, memristances of the 2-synapse can be trained separately and share one training circuit. Fig.12(b) shows a training sharing distribution circuit, which generates training signals to control M_1 and M_2 . The training sharing circuit operations under different conditions are shown in Table 7.

The two synapse inputs A_1 and A_2 can be used to determine which memristor, M_1 or M_2 , is in training. Table 8 lists the required A_1 and A_2 , when the logic functionality of N is one of the following: OR/NOR, XOR/XNOR, AND/NAND.

Compared to the separated training circuit for each memristor, the shared scheme can reduce 26% of training circuit transistor count. More saving in cost and area can be obtained when utilizing this training sharing distribution scheme to multi-synapse structure with more inputs.

6.2.4 Self-Training Mode

To improve training time and reduce power consumption, we introduce the concept of self-training in our design: rather than using a fixed long training period (i.e., 51ms), the self-training mode automatically stop programming memristor whenever V_{out} and D_{train} become same.

The proposed training circuit supports self-training mode by dividing a long training period into multiple shorter periods and detecting V_{out} in between. The programming period needs to be carefully selected: if it is too short, the delay and

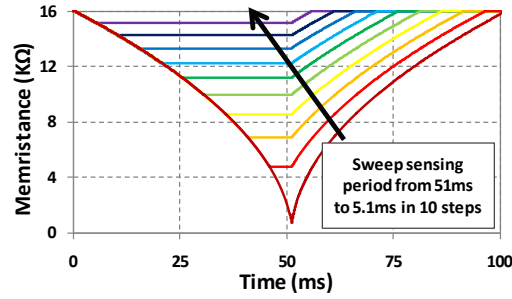


Fig. 13 Self-training simulation.

energy overheads induced by V_{out} detection may overwhelm the benefit of self-training. On the contrary, a long programming period cannot show enough benefit.

The simulation result in Fig. 13 shows the memristance changing when sweeping programming period from 5.1ms to 51ms in 10 steps. Obviously, the self-training mode could significantly reduce training time. In theory, the proposed training circuit can train the memristance to any value between R_H and R_L . The real training time is determined by the specific application and neuron functionality.

7 Conclusion

In this work, we evaluate the impact of different geometry variations on the electrical properties of two different types of memristors, TiO_2 -based memristors and spintronic memristors, by conducting analytic modeling analysis and Monte-Carlo simulations. We investigate the different responses of the static and memristive parameters of the two memristors under various process variations and analyze their implication for the electrical properties of the memristors. A simple LER sample generation algorithm is also proposed to speed up the related Monte-Carlo simulations. At the end, we propose a memristor-based synapse that can be used in neuromorphic computing architecture. The corresponding training operations including multi-synapse schemes and self-training have also been explored and discussed. The proposed synapse design can be generalized to other memristor materials for more applications.

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